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EXAMINER	
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ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/684,328	OHARA ET AL.	
	Examiner	Art Unit	
	Joni Hsu	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-25 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-25 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's arguments with respect to claims 3-5 and 18-20 have been considered but are moot in view of the new ground(s) of rejection.

2. Applicant's arguments, see page 13, line 19-page 14, line 2, filed March 14, 2005, with respect to the rejection(s) of claim(s) 3-5 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Examiner agrees that the offset described in Yutaka (US005664163A) has nothing to do with the amount of data volume that the present application is intended to reduce. Therefore, the rejection has been withdrawn. However, upon further consideration, other prior art can be found to overcome this limitation on new ground(s) of rejection. Baber (US006279041B1) describes that the means for merging comprises a scheduler for judging whether an offset can be performed by merging an increment of data volume caused by a change of drawing commands (Col. 14, lines 49-50; Col. 15, lines 26-35).

3. Applicant's arguments, see page 15, line 17-page 16, line 5, with respect to the rejections of claims 18-20 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Examiner agrees that the uniqueness of the rectangles describes by Pike (US004555775) does not have to do with the data/command transmission from the first apparatus to the second apparatus. Therefore, the rejection has been withdrawn. However, upon further consideration, other prior art can be found to overcome this limitation on new grounds of rejection. Deering

(US005544306A) describes dirty tags, and dirty tags indicate which bits of the buffer have been updated, as is well-known in the art. The dirty tags are employed during block transfer operations between the SRAM buffer (200, Figure 7) and the DRAM banks (Figure 4), and the communication controller (70, Figure 1) performs the transfers (Col. 19, lines 6-25). Therefore, the communication controller transfers only updated areas on a frame memory in a form of commands from the first apparatus (200) to the second apparatus (DRAM banks) (Col. 19, lines 6-25).

4. Applicant's arguments regarding claims 1, 2, 6-17, and 21-25 have been fully considered but they are not persuasive.

5. With regard to claim 1, Applicant argues that there is a lack of motivation to combine Yutaka (US005664163A) and Peaslee (US005265203A) to arrive at the claimed invention (page 11, lines 8-10).

In reply, the Examiner disagrees. It would be obvious to modify the device of Yutaka so that the scheduler merges the data in accordance with the mutual dependency of the instructions among themselves as suggested by Peaslee because Peaslee suggests that the data that are dependent on each other cannot be transferred at the same time (Col. 5, lines 54-59).

6. With regard to claim 2, Applicant argues that Yutaka and Peaslee do not disclose or suggest a means for merging (page 12, lines 8-11).

In reply, the Examiner disagrees. Peaslee discloses a scheduler, which Peaslee calls a cogenerator (10, Figure 1), for merging a plurality of transfer data (Col. 3, lines 19-23). The cogenerator has a multiprocess scheduler (12, Figure 2; Col. 5, lines 5-12) that prevents the subsystems from using the same output at the same time, which means that the data must be merged in such a way that they are not depending on the same output, which means that the data is merged in accordance with the mutual dependency of the instructions among themselves (Col. 5, lines 50-59).

7. With regard to claims 7 and 11, Applicant argues that for somewhat similar reasons as those set forth with respect to claim 1, Applicant submits that Yutaka and Peaslee do not disclose or suggest all of the features defined by claims 7 and 11 (page 14, lines 6-9).

In reply, the Examiner disagrees, for the same reasons given with regard to claim 1.

8. With regard to claims 15-17, Applicant argues that Zhao's (US006405267B1) method is different from the merging operations that the present applicant provides (page 14, line 10-page 15, line 10).

In reply, the Examiner disagrees. Zhao describes generating a plurality of drawing instructions to be transferred from the first apparatus (CPU) to the second apparatus (graphics device) (Col. 1, lines 21-30) by ordering the drawing instructions (Col. 2, lines 43-59) by putting the drawing instructions into slots in the storage buffers, the slot selected based on portions of the address information associated with the data item. The data in the storage buffers is then provided to a command interpreter for further processing by the graphics device (Col. 3, lines

21-35). Therefore, Zhao discloses combining or merging an effect of a plurality of drawing instructions which affect a same area. The storage buffers receive these drawing instructions from the FIFO, which outputs the drawing instructions at graphics device clock rate (Col. 3, lines 21-35). This means that the drawing instructions that are combined or merged which affect a same area are effective for a predetermined short period of time on a frame buffer, the predetermined short period of time being in accordance with the graphics device clock rate. Thus, Zhao describes the elements of claims 15-17 as they are stated in claims 15-17.

9. With regard to claims 21-24, in response to applicant's argument that the combination of the devices of Yutaka and Peaslee with the system configuration of Epard (US005241625A) would not provide the advantages that the claimed combination of the present application is intended to provide (page 16, lines 15-21), a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 370 F.2d 576, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 312 F.2d 937, 939, 136 USPQ 458, 459 (CCPA 1963). The combination of the devices of Yutaka and Peaslee with the system configuration of Epard discloses the limitations of claims 21-24, and therefore is capable of performing the intended use, and therefore meets the claims.

Applicant also argues that it would not have been obvious to combine Yutaka, Peaslee, and Epard (page 17, lines 1-2).

In reply, the Examiner disagrees. It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Yutaka and Peaslee to include a first drawing engine and the second apparatus includes a second drawing engine as suggested by Epard because Epard suggests that in order for the first apparatus to transfer image data to the second apparatus, the first apparatus must have a drawing engine to first process the image data. In order for the second apparatus to display this image data, it must also have a drawing engine (Col. 3, lines 5-43; Col. 48, lines 26-57).

It also would have been obvious modify the devices of Yutaka and Peaslee so that the first apparatus and the second apparatus include redundant drawing engines as suggested by Epard because Epard suggests that the second apparatus is to display the same image data as that of the first apparatus. Therefore, the first apparatus and the second apparatus must include redundant drawing engines (Col. 3, lines 5-43).

It also would have been obvious to modify the devices of Yutaka and Peaslee so that the first apparatus comprises a computer including a first drawing engine, and wherein the second apparatus comprises a display apparatus including a second drawing engine as suggested by Epard because Epard suggests that the first apparatus must comprise a computer in order to process the image data, and the second apparatus must comprise a display apparatus in order to display the information (Col. 3, lines 5-44; Col. 48, lines 26-57).

It also would have been obvious to modify the devices of Yutaka and Peaslee so that the first drawing engine and the second drawing engine each include a dedicated frame memory unit as suggested by Epard because Epard suggests that both the first drawing engine and the second

drawing engine need a dedicated frame memory unit to store image data that is processed by the drawing engines (Col. 48, lines 26-57).

10. With regard to claim 25, Applicant argues that it would not have been obvious to combine Yutaka, Peaslee, Epard, and Nitta (US006392619B1) (page 17, lines 9-12).

In reply the Examiner disagrees. It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Yutaka, Peaslee, and Epard so that the first drawing engine and the second drawing engine generate identical images including a different timing due to a data transfer delay from the first apparatus to the second apparatus as suggested by Nitta because Nitta suggests that there is a data transfer delay from the first apparatus to the second apparatus, so the data transfer delay must be accounted for with a different timing in order to have correct timing (Col. 10, lines 59-67).

In response to applicant's argument that the device of Nitta (US006392619B1) provides the solution of a reduction in the power consumption of data lines between the first apparatus and the second apparatus, not a reduction in the data/command traffic (page 18, lines 5-7), a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 370 F.2d 576, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 312 F.2d 937, 939, 136 USPQ 458, 459 (CCPA 1963). Nitta describes that the data transfer delay allows the first apparatus to merge certain graphics

commands and hold the commands in the first apparatus until the communication link becomes ready to transmit the command to the second apparatus, and this has the advantage of reducing the power consumption (Col. 1, line 53-Col. 2, line 3), but this structure is capable of performing the intended use of the claimed invention, and therefore it meets the claim.

In response to applicant's argument that the examiner has combined an excessive number of references, reliance on a large number of references in a rejection does not, without more, weigh against the obviousness of the claimed invention. See *In re Gorman*, 933 F.2d 982, 18 USPQ2d 1885 (Fed. Cir. 1991).

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

13. Claims 1, 2, 6-10, and 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yutaka (US 5,664,163) in view of Peaslee (US 5,265,203).

14. With regard to Claim 1, Yutaka discloses a data transferring apparatus for transferring transfer packets each including one or more transfer data as objectives of transfer from a first apparatus (42, 43, 45, Figure 1) to a second apparatus (61), each transfer data including commands indicated processes against a preliminarily assigned area, the first apparatus including a scheduler for merging a plurality of the transfer data (43; Col. 6, lines 65-67; Col. 7, lines 1-13), and a communication controller (42) for generating transfer packets each including at least one of one or more transfer data whose amount is within a certain predetermined range (Col. 2, line 15) and one or more merged transfer data (Col. 3, lines 1-8, 25-28), the communication controller transferring the generated transfer packets to the second apparatus (45; Col. 3, lines 12-14).

Yutaka, however, is silent as to whether the plurality of transfer data merged by the scheduler is merged by meeting a certain requirement. According to the disclosure of this

application, the certain requirement that is met is that the scheduler merges the data in accordance with the mutual dependency of the instructions among themselves (Page 15, lines 13-18). However, Peaslee discloses a scheduler, which Peaslee calls a cogenerator (10, Figure 1), for merging a plurality of transfer data (Col. 3, lines 19-23). The cogenerator has a multiprocess scheduler (12, Figure 2; Col. 5, lines 5-12) that prevents the subsystems from using the same output at the same time, which means that the data must be merged in such a way that that they are not depending on the same output, which means that the data is merged in accordance with the mutual dependency of the instructions among themselves (Col. 5, lines 50-59).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Yutaka so that the scheduler merges the data in accordance with the mutual dependency of the instructions among themselves as suggested by Peaslee because Peaslee suggests that the data that are dependent on each other cannot be transferred at the same time (Col. 5, lines 54-59).

15. With regard to Claim 2, Claim 2 is the same as Claim 1, except that Claim 2 does not have specific names for the scheduler and the communication controller, so Yutaka and Peaslee also disclose Claim 2.

16. With regard to Claim 6, Yutaka discloses that the first apparatus comprises a computer (Col. 1, lines 9-14) and the second apparatus comprises a display apparatus (65, Figure 1).

17. With regard to Claims 7-10, Claims 7-10 are the same as Claims 2-4 and 6, except that Claims 7-10 are for a method instead of an apparatus. Yutaka discloses both the data transferring method (Col. 2, lines 46-62) and its apparatus. The details of the method can be seen in Figure 11, steps 101-109, and are described in Col. 11, lines 31-67; Col. 12, lines 1-37. The details for the method for changing the drawing commands if the judging judges that the offset is possible, with regard to Claim 9, can be seen in Figure 4C; Col. 9, lines 38-51.

Peaslee also discloses both the apparatus and method. Figure 3 illustrates the method of how the multiprocess scheduler operates and Figure 4 illustrates the method of the task control functions. Figures 3 and 4 are described in Col. 5, line 48 to Col. 8, line 6.

18. With regard to Claims 11-14, Claims 11-14 are the same as Claims 7-10, except that Claims 11-14 are for a medium for mediating a program to be executed on a computer. The method (101-109, Figure 11; Col. 11, lines 31-67; Col. 12) disclosed by Yutaka is a program that is executed on a computer (42, Figure 1; Col. 11, lines 31-34), so Yutaka discloses a medium for mediating this program to be executed on a computer.

Peaslee discloses a programmable scheduler (Col. 1, lines 31-35), so the method (Figures 3 and 4; Col. 5, line 48- Col. 8, line 6) is a program. Peaslee also suggests that the program is executed on a computer (Col. 1, lines 48-53), so Peaslee discloses a medium for mediating a program to be executed on a computer.

19. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yutaka (US 5,664,163) in view of Peaslee (US 5,265,203), further in view of Barber (US006279041B1).

20. With regard to Claim 3, Yutaka and Peaslee are relied upon for the teachings as discussed above relative to Claim 2.

However, Yutaka and Peaslee do not teach that the means for merging comprises a scheduler for judging whether an offset can be performed by merging an increment of data volume caused by a change of drawing commands. However, Baber describes that the means for merging comprises a scheduler for judging whether an offset can be performed by merging an increment of data volume caused by a change of drawing commands (Col. 14, lines 49-50; Col. 15, lines 26-35).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Yutaka and Peaslee so that the means for merging comprises a scheduler for judging whether an offset can be performed by merging an increment of data volume caused by a change of drawing commands as suggested by Baber because Baber suggests the advantage of minimizing data transfer volume (Col. 14, lines 23-50).

21. With regard to Claim 4, Yutaka and Peaslee do not teach that if the scheduler judges that the offset is possible, then the scheduler changes the drawing commands. However, Baber describes processing a buffer until detecting an end of file indication (Col. 17, lines 29-44). Therefore, the scheduler judges that the offset is possible until detecting an end of file indication (Col. 15, lines 26-35). If additional segments are still contained in the receive buffer and an offset is possible, then the operations return and resume with the next segment from the buffer. Processing the next segment from the buffer inherently includes changing the drawing

commands. Therefore, if the scheduler judges that the offset is possible, then the scheduler changes the drawing commands (Col. 17, lines 29-44).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Yutaka and Peaslee so that if the scheduler judges that the offset is possible, then the scheduler changes the drawing commands as suggested by Baber because Baber suggests that the scheduler needs to make sure that there is enough room left in the file before changing the drawing commands and processing the next segment from the buffer (Col. 17, lines 29-44).

22. With regard to Claim 5, Yutaka discloses that the means for generating comprises a communication controller which generates the transfer packets which contain merged drawing commands which are more than a predetermined data volume in quantity (Col. 2, lines 32-33; Col. 4, lines 5-8).

23. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yutaka (US 5,664,163) in view of Peaslee (US 5,265,203), further in view of Zhao (US006405267B1).

24. With regard to Claim 15, Yutaka and Peaslee are relied upon for the teachings as discussed above relative to Claim 1.

However, Yutaka and Peaslee do not teach that the scheduler generates a plurality of drawing instructions to be transferred from the first apparatus to the second apparatus by combining an effect of a plurality of drawing instructions which affect a same area in a

predetermined short period of time on a frame buffer. However, Zhao describes generating a plurality of drawing instructions to be transferred from the first apparatus (CPU) to the second apparatus (graphics device) (Col. 1, lines 21-30) by ordering the drawing instructions (Col. 2, lines 43-59) by putting the drawing instructions into slots in the storage buffers, the slot selected based on portions of the address information associated with the data item. The data in the storage buffers is then provided to a command interpreter for further processing by the graphics device (Col. 3, lines 21-35). Therefore, Zhao discloses combining or merging an effect of a plurality of drawing instructions which affect a same area. The storage buffers receive these drawing instructions from the FIFO, which outputs the drawing instructions at graphics device clock rate (Col. 3, lines 21-35). This means that the drawing instructions that are combined or merged which affect a same area are effective for a predetermined short period of time on a frame buffer, the predetermined short period of time being in accordance with the graphics device clock rate.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Yutaka and Peaslee so that the scheduler generates a plurality of drawing instructions to be transferred from the first apparatus to the second apparatus by combining an effect of a plurality of drawing instructions which affect a same area in a predetermined short period of time on a frame buffer as suggested by Zhao because Zhao suggests the advantage of increasing effect bus bandwidth (Col. 2, lines 43-59).

25. With regard to Claim 16, Claim 16 is similar in scope to Claim 15, and therefore is rejected under the same rationale.

26. With regard to Claim 17, Claim 17 is similar in scope to Claim 15, and therefore is rejected under the same rationale.

27. Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yutaka (US 5,664,163) in view of Peaslee (US 5,265,203), further in view of Deering (US005544306A).

28. With regard to Claim 18, Yutaka and Peaslee are relied upon for the teachings as discussed above relative to Claim 1.

However, Yutaka and Peaslee do not teach that the communication controller transfers only updated areas on a frame memory in a form of drawing commands to the second apparatus. However, Deering describes dirty tags, and dirty tags indicate which bits of the buffer have been updated, as is well-known in the art. The dirty tags are employed during block transfer operations between the SRAM buffer (200, Figure 7) and the DRAM banks (Figure 4), and the communication controller (70, Figure 1) performs the transfers (Col. 19, lines 6-25). Therefore, only the updated areas on a frame memory are transferred in a form of drawing commands from the first apparatus (200) to the second apparatus (DRAM banks) (Col. 19, lines 6-25).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Yutaka and Peaslee so that the communication controller transfers only updated areas on a frame memory in a form of drawing commands to the second apparatus as suggested by Deering because it inherently avoids unnecessary transfers and therefore saves processing resources (Col. 19, lines 6-25).

29. With regard to Claim 19, Claim 19 is similar in scope to Claim 18, and therefore is rejected under the same rationale.

30. With regard to Claim 20, Claim 20 is similar in scope to Claim 18, and therefore is rejected under the same rationale.

31. Claims 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yutaka (US 5,664,163) in view of Peaslee (US 5,265,203), further in view of Epard (US005241625A).

32. With regard to Claim 21, Yutaka and Peaslee are relied upon for the teachings as discussed above relative to Claim 2.

However, Yutaka and Peaslee do not teach that the first apparatus includes a first drawing engine and the second apparatus includes a second drawing engine. However, Epard describes that the first apparatus (50, Figure 5A) includes a first drawing engine (55) and the second apparatus (60) includes a second drawing engine (61) (Col. 48, lines 26-57).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Yutaka and Peaslee to include a first drawing engine and the second apparatus includes a second drawing engine as suggested by Epard because Epard suggests that in order for the first apparatus to transfer image data to the second apparatus, the first apparatus must have a drawing engine to first process the image data. In order for the

second apparatus to display this image data, it must also have a drawing engine (Col. 3, lines 5-43; Col. 48, lines 26-57).

33. With regard to Claim 22, Yutaka and Peaslee do not teach that the first apparatus and the second apparatus include redundant drawing engines. However, Epard describes that the first apparatus (50, Figure 5A) and the second apparatus (60) display the same information (Col. 3, lines 5-43). Therefore, Epard describes that the first apparatus and the second apparatus include redundant drawing engines (55, 61) because both drawing engines process the same information.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Yutaka and Peaslee so that the first apparatus and the second apparatus include redundant drawing engines as suggested by Epard because Epard suggests that the second apparatus is to display the same image data as that of the first apparatus. Therefore, the first apparatus and the second apparatus must include redundant drawing engines (Col. 3, lines 5-43).

34. With regard to Claim 23, Yutaka and Peaslee do not teach that the first apparatus comprises a computer including a first drawing engine, and wherein the second apparatus comprises a display apparatus including a second drawing engine. However, Epard describes that the first apparatus (50, Figure 5A) comprises a computer including a first drawing engine (55), and wherein the second apparatus (60) comprises a display apparatus (65) including a second drawing engine (61) (Col. 3, lines 5-44; Col. 48, lines 26-57).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Yutaka and Peaslee so that the first apparatus comprises a computer including a first drawing engine, and wherein the second apparatus comprises a display apparatus including a second drawing engine as suggested by Epard because Epard suggests that the first apparatus must comprise a computer in order to process the image data, and the second apparatus must comprise a display apparatus in order to display the information (Col. 3, lines 5-44; Col. 48, lines 26-57).

35. With regard to Claim 24, Yutaka and Peaslee do not teach that the first drawing engine and the second drawing engine each include a dedicated frame memory unit. However, Epard describes the first drawing engine (55, Figure 5A) and the second drawing engine (61) each include a dedicated frame memory unit (57, 65; Col. 48, lines 26-57).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Yutaka and Peaslee so that the first drawing engine and the second drawing engine each include a dedicated frame memory unit as suggested by Epard because Epard suggests that both the first drawing engine and the second drawing engine need a dedicated frame memory unit to store image data that is processed by the drawing engines (Col. 48, lines 26-57).

36. Claims 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yutaka (US 5,664,163) in view of Peaslee (US 5,265,203), further in view of Epard (US005241625A0), further in view of Nitta (US006392619B1).

Yutaka, Peaslee, and Epard are relied upon for the teachings as discussed above relative to Claim 21. Epard describes that the first drawing engine and the second drawing engine generate identical images, as discussed in the rejection for Claim 22.

However, Yutaka, Peaslee, and Epard do not teach that the first drawing engine and the second drawing engine generate identical images including a different timing due to a data transfer delay from the first apparatus to the second apparatus. However, Nitta describes the data transfer of images for which the same data is continuously transferred (Col. 9, lines 7-10), meaning that the first apparatus and the second apparatus generate identical images. Nitta describes a different timing due to a data transfer delay from the first apparatus to the second apparatus (Col. 10, lines 59-67).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Yutaka and Peaslee so that the first drawing engine and the second drawing engine generate identical images including a different timing due to a data transfer delay from the first apparatus to the second apparatus as suggested by Nitta because Nitta suggests that there is a data transfer delay from the first apparatus to the second apparatus, so the data transfer delay must be accounted for with a different timing in order to have correct timing (Col. 10, lines 59-67).

37. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Vegesna (US 5,640,588) teaches a scheduler (2, Figure 18) for merging a plurality of transfer data in accordance with the mutual dependency of the instructions among themselves

(Col. 3, lines 12-37; Col. 23, lines 6-20). Vegesna also teaches that when there are data dependencies between instructions, they cannot be issued simultaneously (Col. 33, lines 38-40), and Vegesna suggests the advantage of achieving multiple launches and executions of the instructions by merging the data in accordance with the mutual dependency of the instructions among themselves (Col. 3, lines 12-37). Vegesna discloses both the apparatus and method (Col. 1, line 12). The details of the method for merging a plurality of transfer data in accordance with the mutual dependency of the instructions among themselves are described in Col. 26, lines 4-62.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew C. Bella can be reached on 571-272-7778. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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